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BEFORE THE BOARD OF PATENT APPEALS
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Paper No. 32

Application Number: 09/000,626
Filing Date: December 30, 1997
Appellant(s): RENGARAJAN ET AL.

Stanton C. Braden
For Appellant

RESPONSE TO REMAND

Copies of English language translation of Japanese reference 57-159038 obtained from STIC Translations Branch have been placed in the record and a copy of translation has been sent to Applicant.

It was an inadvertently mistake in the examiner's answer to include claims 2-5, 7 and 25 in the 35 U.S.C. 112 rejection. Claims 2-5, 7 and 25 are now removed from the 112 rejection in the examiner's answer so that only claims 1 and 24 are rejected under 35 U.S.C. 112, 1st paragraph.

Correction of the physical entry of Amendment C has been done.

Tom Thomas

TOM THOMAS
SUPERVISOR
TECHNICAL EXAMINER
FEB 11 2000

Japanese Published Unexamined (Kokai) Patent Application No. S57-159038, published October 1, 1982; Application No. S56-43800, filed March 25, 1981; Int. Cl.³: H01L 21/76 21/302 21/318; Inventor(s): Takeshi Fukuda et al.; Assignee: Fujitsu Corporation; Japanese Title: Buijigata Bunriryoudiki no Keiseihouhou (Method for Formation of a V-Shaped Separation Area)

1. Title of Invention

Method for Formation of a V-Shaped Separation Area

2. Claim

A method for formation of a V-shaped separation area, characterized in that, after a groove with a V-shaped cross-section has been formed onto a semiconductor substrate so as to be at a depth reaching at least a P type semiconductor area, a silicon oxide film and a silicon nitride film are formed onto the side wall of said V-shaped groove in the order; next, said silicon oxide film inside said V-shaped groove is removed except for a location around the bottom of said V-shaped groove; after this, the inside of the V-shaped groove is filled with polycrystalline silicon.

3. Detailed Description of the Invention

This invention pertains to the formation of V-shaped isolation areas on semiconductor substrates; in particular, this invention pertains to the formation of V-shaped isolation areas without generating n type inversion layers to p type substrate areas that are adjacent to the bottoms of V-shaped grooves.

As for mainly the formation of bipolar type integrated circuits, grooves with V-shaped cross-section are formed to substrate crystal wherein {100} surfaces are used as main surfaces in the $\langle 110 \rangle$ direction. Since said V-shaped grooves are used for the purpose of dividing n type layers on the substrate surfaces, they are formed at the depth reaching p type areas under said grooves.

On the other hand, in order to make the substrate surfaces flat, said V-shaped grooves are filled with polycrystalline silicon (henceforth refers to as poly Si); however, silicon dioxide (SiO_2) films are provided between the side walls of V-shaped grooves and poly Si.

As for said structure, if SiO_2 films which are in contact with p type substrates are contaminated by Na^+ ions, n type inversion areas are generated to p type areas; as a result, the separation between device areas becomes incomplete. As for a method to prevent said incompleteness, areas which are in contact with the bottoms of V-shaped grooves are transformed into p^+ types; by means of this, the generation of inversion layers is prevented; however, as for an easier method, the surfaces of SiO_2 films inside V-shaped grooves are covered with silicon nitride (Si_3N_4) films; by means of this, Na^+ ions are blocked.

Problems of said method is as below. As shown in Fig.1, an n type layer 2 is presented onto a p type silicon substrate 1 (henceforth refers to as a Si substrate); a V-shaped groove is engraved onto n type layer 2; a SiO_2 film 3 is adhered onto the side wall. When a Si_3N_4 film 4 is further formed by an adhesion means continuously from the horizontal surface of the substrate to the side surface of the V-shaped groove, as Si_3N_4 film 4 at the horizontal surface section of the substrate is removed in order to form a device, as shown in Fig.2, the Si_3N_4 film is excessively etched off; as a result, a small groove 7 is created. Said small groove causes

damage including the cutting of the wire of a wiring layer; because of that, said formation has to be avoided as much as possible.

This is the same as the formation of the end of a Si_3N_4 film at the horizontal section as shown in Fig.3; an overhang 7' occurs; as a result, said overhang 7' causes the cutting of a wiring. In the drawing, reference number 5 refers to a poly Si; reference number 6 refers to a SiO_2 area.

Accordingly, when Na^+ ions are blocked using a Si_3N_4 film, it is necessary to form only at a desired section and not to extend to the substrate surface.

Also, as for an exposure means, called a proximity, it is possible to provide a mask distant from a photosensitive layer at several ten μ and to transfer a sharp image. Positioning margin at 1 μm is not so a severe condition due to the advancement of positioning technologies.

Thus, by using said exposure technology, the present invention selectively forms a Si_3N_4 film at an about 3 μm width inside a V-shaped groove at an about 6 μm width in the horizontal direction. More specifically, the present invention is characterized in that, after a groove with a V-shaped cross-section has been formed onto a semiconductor substrate so as to be at a depth reaching at least a p type semiconductor area, a SiO_2 film and a Si_3N_4 film are formed onto the side wall of said V-shaped groove in the order; next, said silicon oxide film inside said V-shaped groove is removed except for a location around the bottom of said V-shaped groove; that, after this, the inside of the V-shaped groove is filled with polycrystalline silicon.

Fig.4 illustrates steps as in an embodiment of the present invention. First, as shown in Fig.4 (a), the surface of a Si substrate 10 is covered with a SiO_2 film 11 and a Si_3N_4 film 12; a V-shaped groove forming window 13 is opened. Next, after a V-shaped groove has been formed

by an etching means, the surface inside the groove is covered with a SiO_2 film 11' [Fig.4 (b)]. When SiO_2 film 11' is formed by a thermal oxidation means, a CVD SiO_2 film is formed onto Si_3N_4 film 12 in advance; a patterning is applied to three layers consisting of SiO_2 , Si_3N_4 , and CVD SiO_2 . The reason for it is that, when a patterning is applied to a Si_3N_4 film to be formed later, initially formed Si_3N_4 film 12 is protected. Also, even though it is not shown in the drawing, it is natural that the V-shaped groove is formed at a depth reaching a p type area inside the substrate.

Next, after a Si_3N_4 film 12' has been formed onto the entire surface of the substrate, a photoresist is applied; by using a non-contact type exposure method such as a proximity method, a photoresist is left only at the bottom of the V-shaped groove. Fig.4 [c] illustrates said process. Following this, using a dry etching means, a patterning is applied to photoresist 14 so as to form a mask; the Si_3N_4 film at locations other than the bottom of the V-shaped groove is removed. Fig.4 (d) illustrates said process.

Because a dry etching can be accommodated with a material to be etched by adjusting the condition, by using said dry etching, it is possible to apply a Si_3N_4 film patterning using a photoresist as a mask. When a SiO_2 film on the side wall of a V-shaped groove is divided into two layers that consist of a CVD film and a thermal oxidation film, films up to a CVD SiO_2 film are removed at said etching process.

After this, the inside of the V-shaped groove is embedded with poly Si; the surface is polished and flattened; the poly Si surface is further oxidized; said oxidized poly Si surface is covered with a SiO_2 film. These are conventional forming steps for a V-shaped groove poly Si separation area [Fig.4 (e)].

As described above, when the present invention is used, it is possible to cover the bottom of a V-shaped groove with a Si_3N_4 film that is not connected to a Si_3N_4 film at the surface section of a substrate; the generation of an n channel at isolation of a poly Si filling type V-shaped groove can be prevented.

4. Brief Description of the Invention

Fig.1 to Fig.3 illustrate prior art forming method; Fig.4 illustrates an embodiment of the present invention; in the drawing, reference number 1 refers to a Si substrate p type area; reference number 2 refers to a Si substrate n type area; reference numbers 3 and 4 refer to SiO_2 ; reference number 4 refers to Si_3N_4 ; reference number 5 refers to poly Si; reference number 7 refers to a groove; reference number 7' refers to an overhang; reference number 10 refers to a Si substrate; reference numbers 11, 11', and 11'' refer to SiO_2 ; reference numbers 12 and 12' refer to Si_3N_4 ; reference number 13 refers to an etching window; reference number 14 refers to a photoresist.

Translations Branch
U.S. Patent and Trademark Office
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Chisato Morohashi